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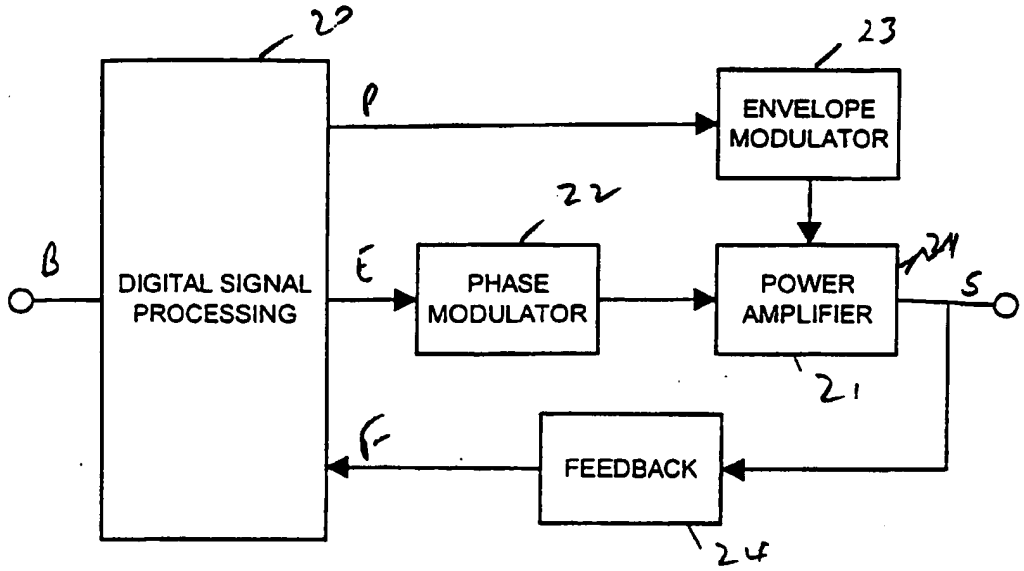
(54) Title: IMPROVEMENTS RELATING TO EER TRANSMITTERS



(57) Abstract: Amplification systems based on EER techniques, generally using digital methods to determine envelope and phase information. Cartesian or predistortion feedback is preferably used to improve a range of characteristics. Envelope modulation may be implemented in various ways such as a sigma delta modulator. Phase modulation may also be implemented in various ways such as a fractional N phase lock loop.

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IMPROVEMENTS RELATING TO EER TRANSMITTERS

FIELD OF THE INVENTION

This invention relates to amplification systems for radio frequency signals and in particular but not solely to envelope elimination and restoration (EER) techniques for radio transmitters. More specifically the invention relates to feedback, and phase or envelope modulation aspects of these techniques. In one embodiment a phase lock loop (PLL) arrangement enables phase modulation and adjustment.

BACKGROUND TO THE INVENTION

Mobile communication systems require high frequency power amplifiers for both base station transmitters and portable units carried by users. These amplifiers operate most efficiently at saturation in the non-linear range of their input/output characteristics. Efficiency is important for battery life and weight in the portable units while linearity is important for base stations with multiple carrier transmission. A number of techniques have been developed to compensate for non-linear amplifier operation. Techniques involving modulation feedback from the amplified signal can be divided in two groups depending on how the modulating signal is represented in the baseband. Cartesian amplification systems apply a feedback signal to quadrature components of the modulating signal. Polar loop amplification systems are based on EER techniques with addition of envelope and phase feedback arrangements. The phase feedback forms a PLL although envelope feedback alone may be used.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide for improved amplification systems based on EER techniques. In general terms the invention may use Cartesian feedback and/or predistortion feedback in these techniques for linearisation. In one embodiment the invention implements a PLL with phase modulation by way of a fractional-N divider.

Accordingly the invention may broadly be said to consist in an amplification system for a radio transmitter comprising: a processing subsystem which determines envelope information and phase information from a baseband input signal, a phase modulator which generates a substantially constant amplitude signal having phase determined by the phase information, an envelope modulator which generates an amplitude modulation signal determined by the envelope information, and an amplifier which generates an output signal from the constant amplitude signal and the amplitude modulation signal.

The phase modulator may include a PLL or other such as a quadrature modulator. The PLL preferably includes a frequency divider which is modulated according to the phase information. Preferably the envelope modulator includes a pulse width modulator or a sigma delta modulator.

The processing subsystem may modify the envelope or phase information according to various forms of Cartesian feedback from the output signal from the amplifier. The processing subsystem may also or alternatively provide a predistort signal to the phase modulator or the envelope modulator in a variety of ways.

The invention may also broadly be said to consist in any alternative combination of features which are suggested in this specification. All equivalents of these features are included.

BRIEF LIST OF FIGURES

Preferred embodiments of the invention will be described with reference to the drawings of which:

Figure 1 schematically shows a radio transmitter with amplification of a signal by a polar loop feedback system,

Figure 2 shows an amplification system in a general form according to the invention,

Figure 3 shows one embodiment of the system with Cartesian feedback,

Figure 4 shows another embodiment of the system with feedback for predistortion,

Figure 5 shows an alternative embodiment of the system with feedback for predistortion,

Figure 6 shows another embodiment with phase modulation by way of a phase lock loop,

Figure 7 shows a PLL arrangement for use in the system of Figure 6,

Figure 8 shows an alternative embodiment using a phase lock loop,

Figure 9 shows a PLL arrangement for use in the system of Figure 8,

Figure 10 shows a digital envelope feedback arrangement,

Figure 11 shows an analog envelope feedback arrangement.

Figures 12, 13, 14 show amplitude modulators in more detail, and

Figure 15 shows a phase modulation arrangement.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to the drawings it will appreciated that the invention may be implemented in various forms and that these embodiments are described by way of example only. Details of existing mobile communication systems will also be known to a skilled reader and need not be given here.

Figure 1 shows EER implemented in a traditional polar loop system. An incoming RF signal I is converted by analog block 10 into polar signals Θ, r respectively containing phase and envelope information. A phase controlled loop including power amplifier 11 operating in saturation then generates an output signal S according to the information, for transmission by antenna 12. The phase controlled loop forms a PLL which receives signal Θ and provides a constant amplitude signal to the non-linear amplifier. A power supply to the amplifier receives signal r and thereby controls gain of the amplifier to restore envelope information and produce signal S. The PLL includes a phase comparator or detector 13 which compares the phases of signal Θ and feedback from signal S to determine the frequency of a voltage controlled oscillator 14. The oscillator in turn provides the constant amplitude signal to the amplifier. Signal r is also modified by addition in block 15 of feedback from signal S. The feedback arrangement includes an optional frequency downconverter 16 followed alternatively for signals Θ, r by an amplitude limiter 16' and envelope detector 17.

Figure 2 gives a schematic overview of the invention in a very general form. A digital sub-system or processor arrangement 20, such as a DSP, determines phase and envelope signals P and E from an incoming signal B. A power amplifier 21 generates an output signal S which contains B modulated on a radio frequency carrier. A phase modulator 22 such as a PLL or quadrature modulator forms a phase modulation path which feeds the amplifier, although in some cases the amplifier may be part of the modulator. An envelope modulation path varies the amplifier gain by way of a modulator 23, which may vary a power supply to one stage of the amplifier for example. The phase and envelope signals P and E may include several components such as predistortion signals as indicated below. A feedback path from the output of the amplifier to the digital sub-system may take many forms, preferably a Cartesian loop which combines with quadrature signals in the digital sub-system. Feedback arrangement 24 may include a range of process components such as an analog detector at the output of the amplifier, an analog-to-digital converter (ADC) for single or quadrature signals from the detector, and other specialised components such as an optimiser for predistortion.

Figure 3 shows one embodiment with several components of the digital sub-system in Figure 2. Baseband signal B is converted to quadrature signals I, Q which are input to a phase extraction process 30 which in turn provides a phase signal for the modulator 22, and input to an envelope detector 31 which provides an envelope signal for the modulator 23. Feedback from the amplifier 21 is processed by a detector 34, ADC 35 and further digital processing stage 36 as may be required before addition to the quadrature signals I, Q at combiners 37, 38. The feedback arrangement therefore forms a Cartesian loop which tends to suppress imperfections in modulation of the amplifier and generally to linearise the amplification process. The loop may be partly or fully analog. Baseband sampling, or low or high intermediate frequency sub-sampling may be used in a partly digital Cartesian loop.

Figures 4 and 5 are other embodiments of Figure 2 involving adaptive predistortion of the quadrature signals I, Q. They also incorporate a feedback arrangement which may or may not be a Cartesian loop such as shown in Figure 3. One advantage of predistortion without a Cartesian loop is the increased stability provided by an open rather than closed loop system. In Figure 4 a digital predistorter 40 determines a

distortion of the quadrature signals before input to the phase extraction and envelope detection stages. In Figure 5 a predistorter 50 determines separate distortion signals for the phase and envelope modulators. An optimisation process depending on the open loop feedback is normally required in each case.

Figure 6 shows another embodiment of an amplification system based on EER according to the invention. Phase and envelope signals P and E are again formed from an input B. A PLL frequency synthesiser 60 containing a frequency divider such as shown in Figure 7 forms a phase modulation path which feeds the amplifier. An envelope modulation path varies the amplifier gain by way of a modulator 61. The digital sub-system also preferably determines a phase offset signal O provided to the PLL over an offset adjustment path as described further below. This provides a fine adjustment of the phase of signal S if required to compensate distortion, and also equalises discrepancies between the phase and envelope modulation paths. A feedback arrangement including detection of envelope and/or phase distortion in signal S preferably provides a feedback signal F for the digital sub-system. A detector and ADC system 24 may be implemented in various ways either separately or incorporated partly in the sub-system. An alternative embodiment in which the amplifier forms part of the PLL is described in Figure 8.

Figure 7 shows a PLL arrangement having a frequency divider which could be used in the embodiment of Figure 6. The arrangement produces an output signal having a frequency which is an integer or fractional multiple of a reference signal and which is modulated according to the phase signal P. A voltage controlled oscillator 70 receives a control signal from phase comparator 71 by way of loop filter 72, and produces a constant amplitude output for the amplifier 21. The loop filter generally integrates an output provided by the comparator according to phase differences between a reference signal from frequency reference 73 and a feedback signal from the controlled oscillator. A phase offset may be introduced between the reference and feedback signals by signal O from the digital sub-system 20, according to feedback from amplifier 21. This may control the action of an additional current source or sink at the input to the loop filter, for example. A frequency divider 74 under control of a modulator 75 introduces phase signal P from the digital sub-system. The modulator is preferably a sigma-delta arrangement which determines

an instantaneous integer value N for the divider in accord with a clock signal from the output of the divider. Signal P forms a digital control word for the modulator.

Figure 8 shows another embodiment of an amplification system based on EER according to the invention. The arrangement is generally similar to that of Figure 6 except that some or all of the stages represented by amplifier 21 and fed by PLL 60 are now included within PLL 90, such as shown in Figure 9. This has an advantage that AM-PM phase errors caused by the amplifier stages are inherently corrected, so that there may be less requirement for a phase adjustment by offset signal O to compensate distortion. The signal may still be required to equalise discrepancies between the phase and envelope modulation paths. Coarse adjustment by a full cycle of the digital sampling period might still be required. On the other hand delay around the loop may be increased with loss of stability and possibly smaller bandwidth. Inclusion of amplification stages introduces additional delay in the loop. The gain and therefore bandwidth must be reduced to maintain stability.

Figure 9 shows a PLL arrangement having a frequency divider which could be used in the embodiment of Figure 8. The arrangement is generally similar to that of Figure 7 except that power amplifier stages 91 being some or all stages of the amplifier 21 in Figure 7, are included in the loop. Envelope information from the digital sub-system 22 is used to modulate the gain of the amplifier stages by way of signal E as before. A limiter 72 is also included to remove the envelope information from signal S before input to the divider 74. The limiter may form part of the input circuitry of the dividers, such as a high gain differential input of the kind found in pre-scalers commonly used in frequency synthesisers.

Figures 10 and 11 show digital and analog systems for obtaining envelope feedback from the power amplifiers 21 or 71 to determine a signal F for the digital sub-system 20. Digital feedback generally requires an envelope detector 100 which may be implemented in many ways. ADC 101 and DAC 102 are also generally required. Typically the amplitude modulator is a switching type to which the digital signal is directly applied. A combination function 105 of the feedback information with envelope information from the incoming signal B may then be used to form signal E for modulation of the amplifier. Analog feedback also requires an envelope

detector 110. A combination function 115 of the feedback with the envelope information takes place outside the digital sub-system before formation of signal E. Further feedback of distortion information may of course be provided by one or more signals F as shown in Figure 2, in addition to or instead of phase or envelope feedback. This would enable pre-distortion of the envelope and phase information signals E and P as described in relation to Figures 4 and 5. Processing to determine channel power or bandwidth effects might be used in signal S, for example.

Figure 12 shows a possible arrangement for linearisation of the amplitude modulator in more detail. Various options are shown in this illustration only some of which may be needed in practice. The power amplifier 120 in this example may be controlled by the modulator 121 by way of supply voltage or DC gate bias, as shown, or both. One or more of the drivers 122 to the amplifier might also be modulated. An envelope detector 123 provides an analog voltage signal from the digital processing sub-system 20 in Figure 2. The signal is mapped as required by a stage 124 to the modulator 121, or to the driver 122 through a digital-to-analog converter (DAC) 125. Localised feedback through ADC 126 can be used to assist linearisation of the modulator 121 if required.

Figures 13 and 14 show two alternatives for the amplitude modulator 23 of Figure 2 in more detail. An analog signal X is input to a pulse width modulator 130 in Figure 13 and a digital signal Y is interpolated to a sigma delta modulator in Figure 14. In both cases the modulator drives a switching transistor 131, 141 through a low pass filter 132, 142 to the amplifier 21. A single loop sigma delta modulator is generally most effective having a large dynamic range, and can be part of an all digital circuit.

Figure 15 show two alternative feedback paths which might be used to linearise the phase modulator 22 of Figure 2. The degree of linearity is generally required to match the AM-PM of the power amplifier 21. Either one or two drivers 151 of the amplifier may be encompassed in feedback. A limiter 150 is typically required in the latter case to remove amplitude modulation.

CLAIMS:

1. An amplification system for a radio transmitter comprising:

a processing subsystem which determines envelope information and phase information from a baseband input signal,

a phase modulator which generates a substantially constant amplitude signal having phase determined by the phase information,

an envelope modulator which generates an amplitude modulation signal determined by the envelope information, and

an amplifier which generates an output signal from the constant amplitude signal and the amplitude modulation signal.

2. A system according to claim 1 wherein:

the phase modulator includes a phase-lock-loop or a quadrature modulator.

3. A system according to claim 1 wherein:

the envelope modulator includes a pulse width modulator or a sigma delta modulator.

4. A system according to claim 2 wherein:

the phase-locked-loop includes a frequency divider which is modulated according to the phase information.

5. A system according to claim 4 wherein:

the frequency divider is modulated by a sigma-delta modulator which is controlled by the processor.

6. A system according to claim 1 wherein:

the processing subsystem modifies the envelope information according to Cartesian feedback from the output signal from the amplifier.

7. A system according to claim 1 wherein:

the processing subsystem modifies the phase information according to Cartesian feedback from the output signal from the amplifier.

8. A system according to claim 1 wherein:

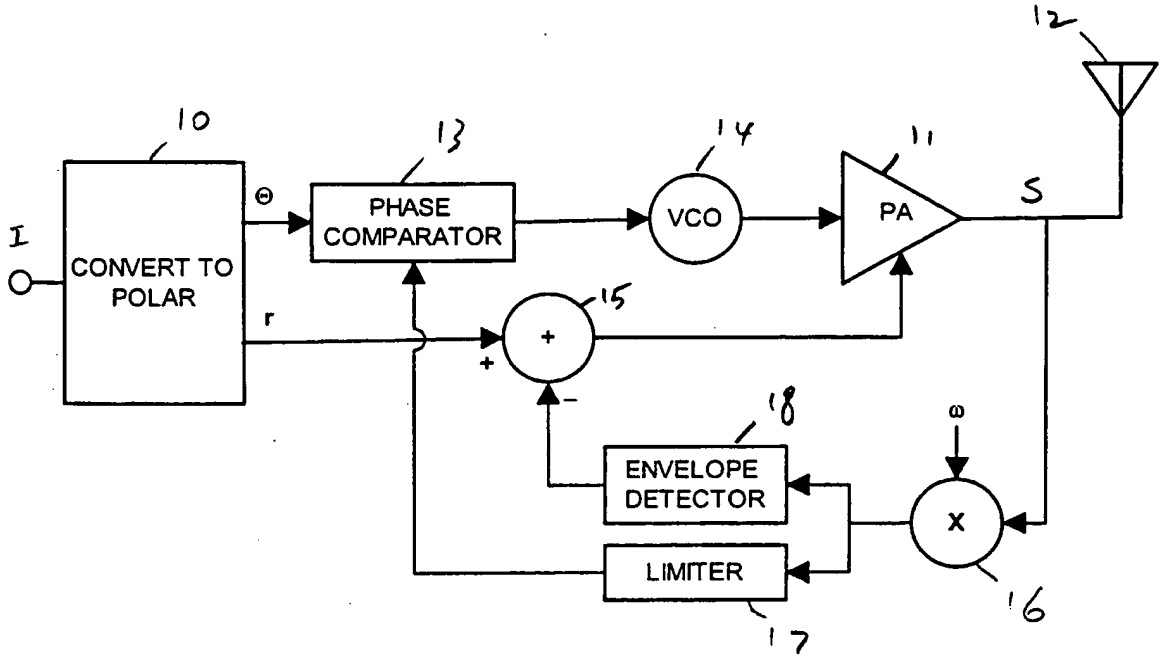
the processing subsystem predistorts the phase modulation of the output signal according to the envelope information and feedback from the output signal.

9. A system according to claim 1 wherein:

the processing subsystem predistorts the phase modulation of the output signal by modifying the phase information.

10. A system according to claim 1 wherein:

the amplifier is part of the phase modulator.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Θ
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18
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ENVELOPE DETECTOR
X
LIMITER
16
17

FIGURE 1

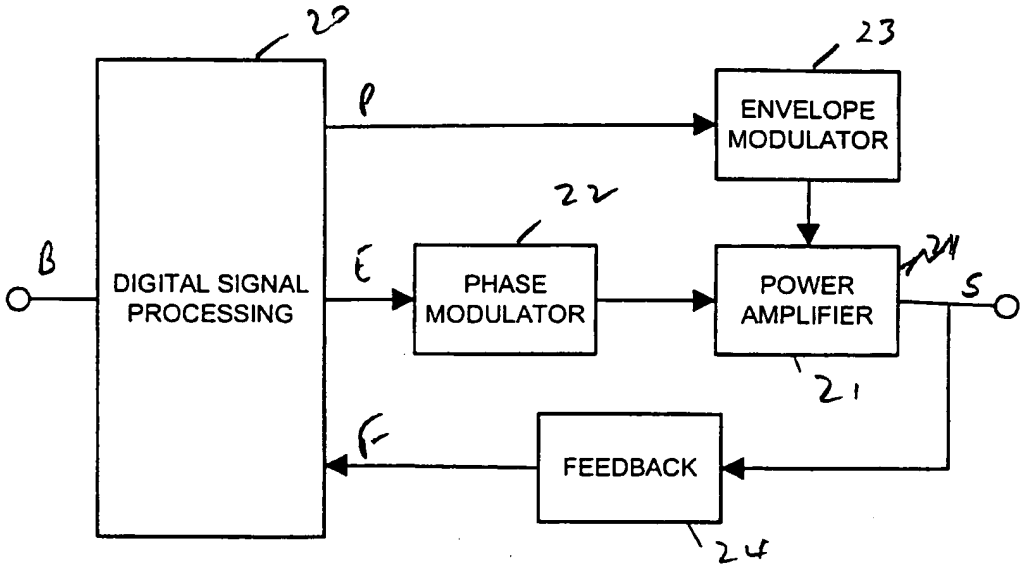

FIGURE 2

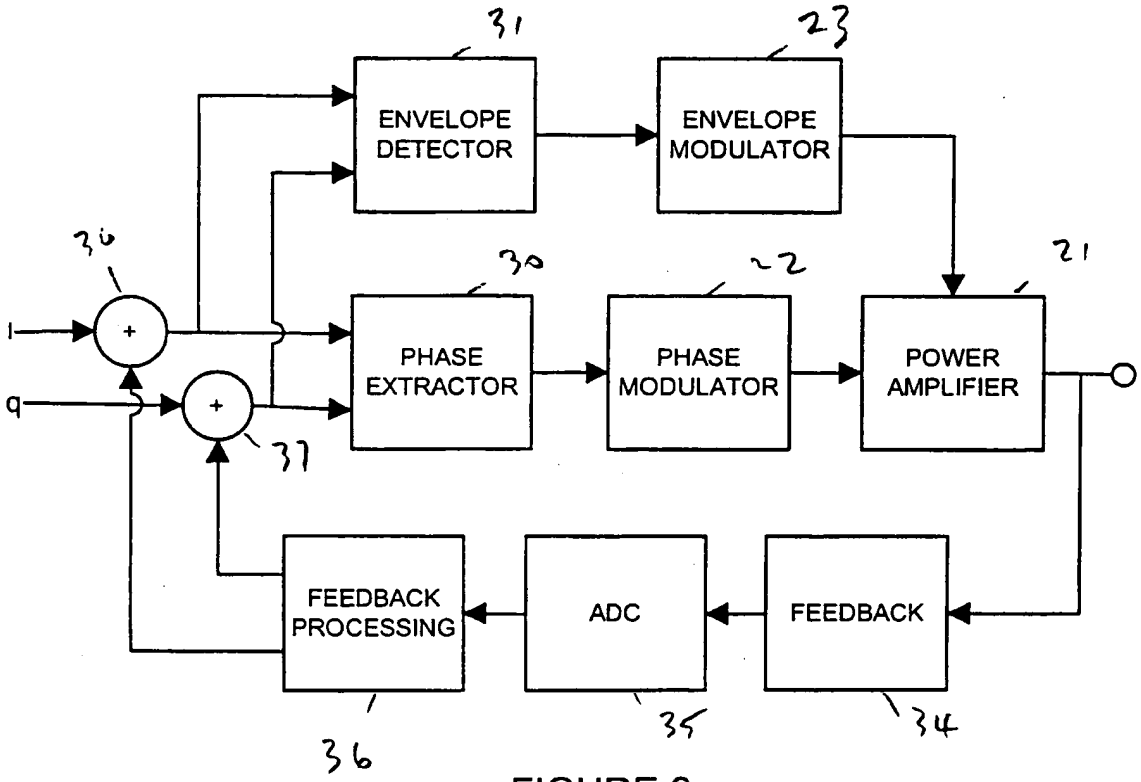

FIGURE 3

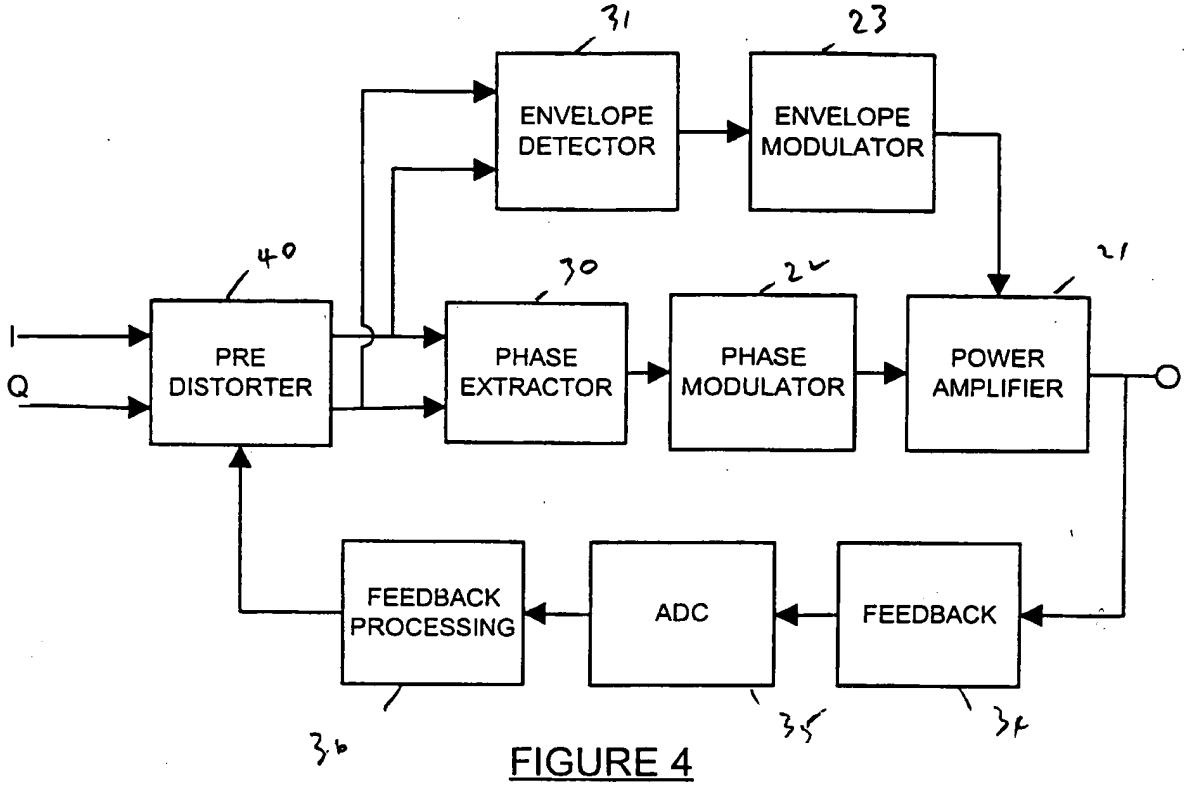

FIGURE 4

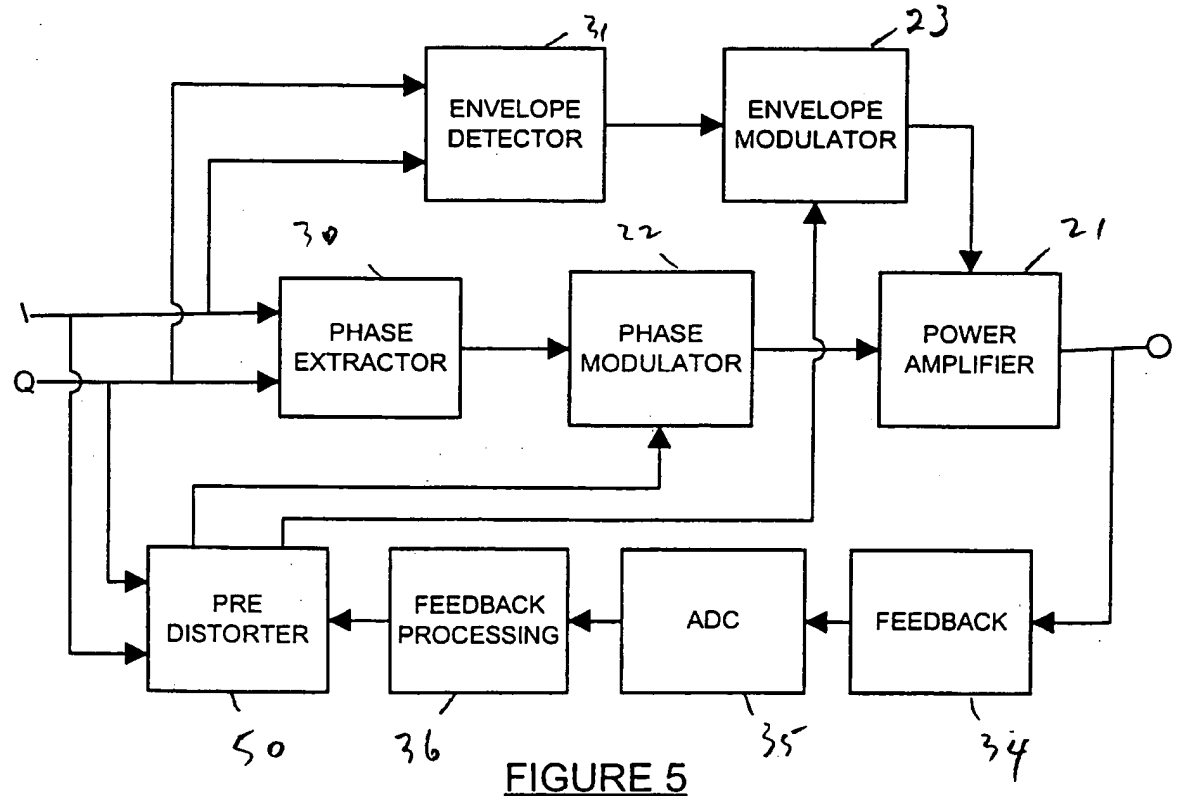

FIGURE 5

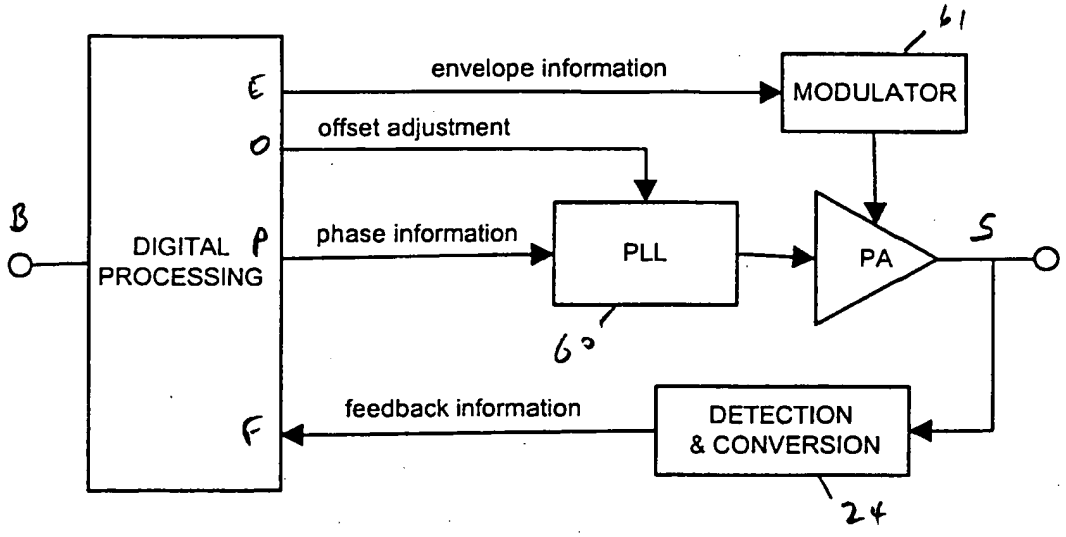

FIGURE 6

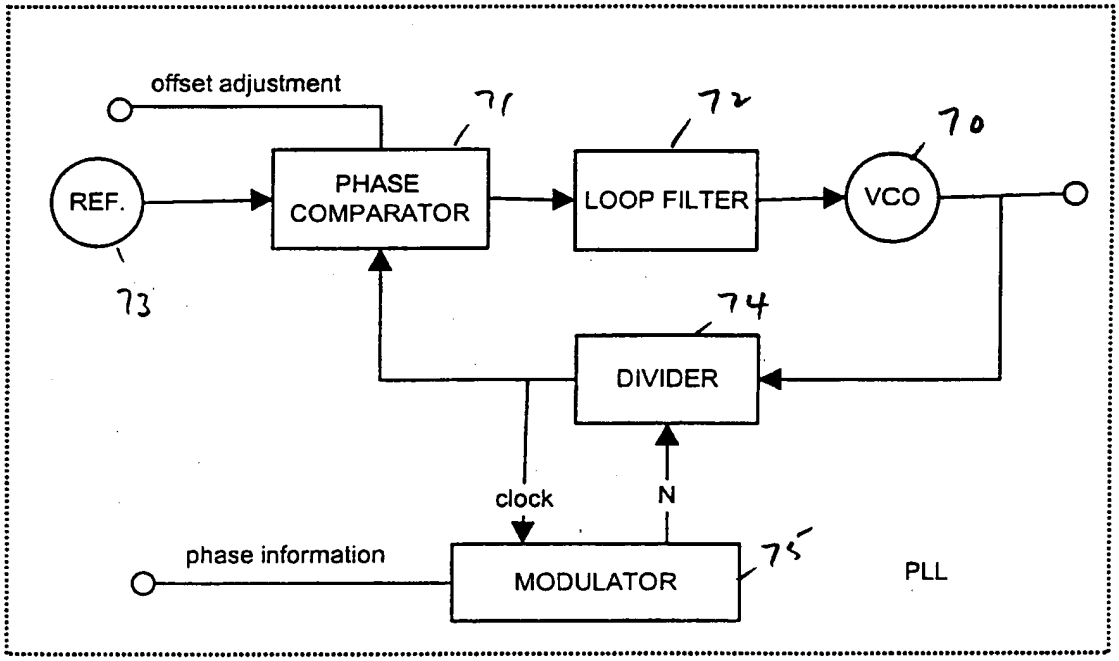

FIGURE 7

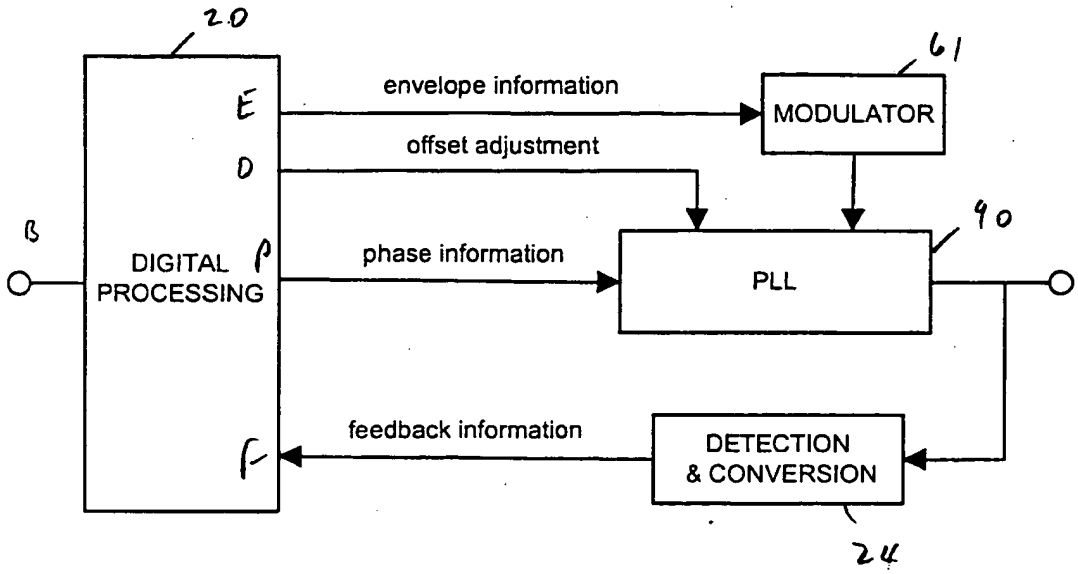

FIGURE 8

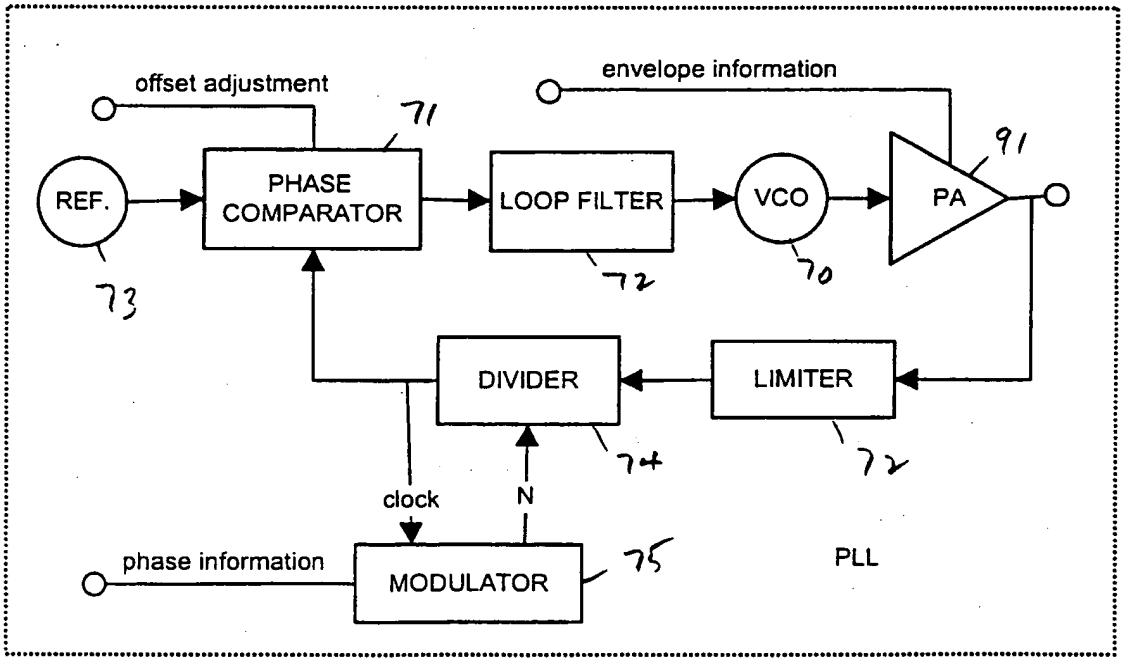

FIGURE 9

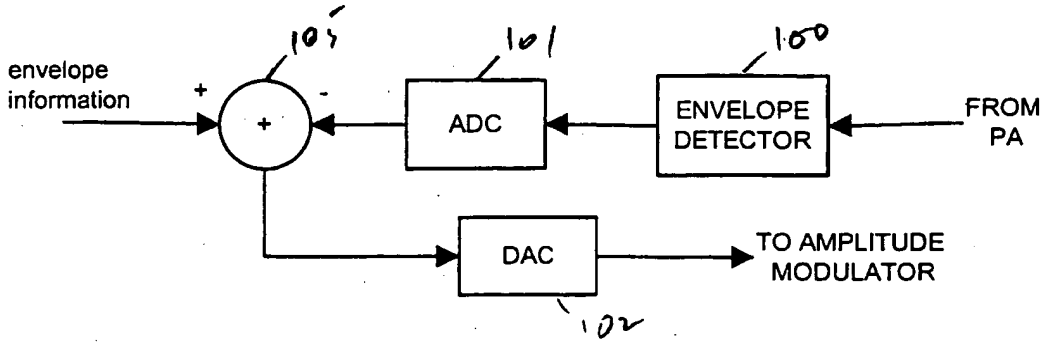

FIGURE 10

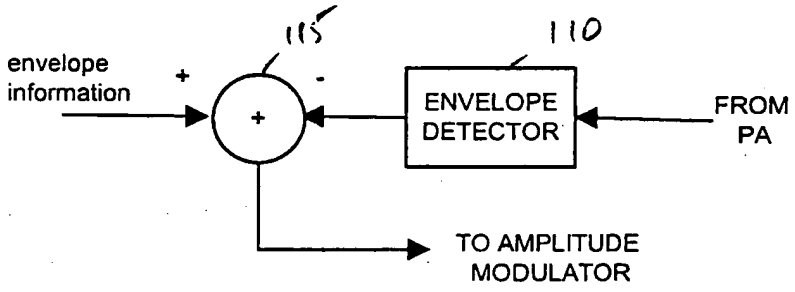

FIGURE 11

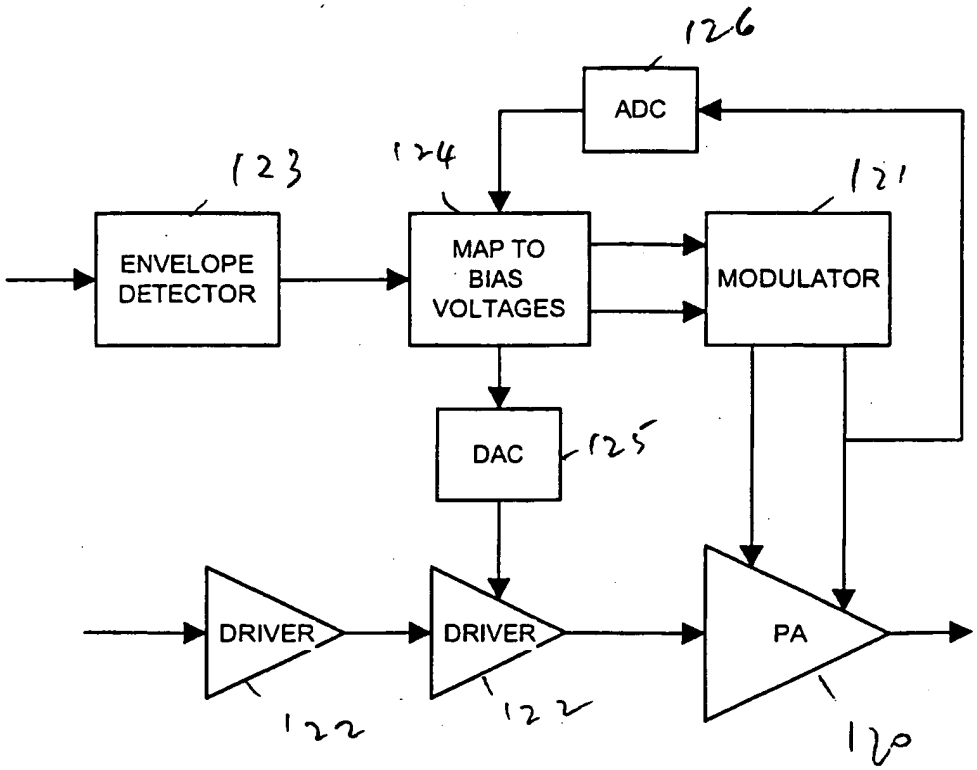
126
ADC
123
124
121
ENVELOPE DETECTOR
MAP TO BIAS VOLTAGES
MODULATOR
DAC
125
DRIVER
DRIVER
PA
122
122
120

FIGURE 12

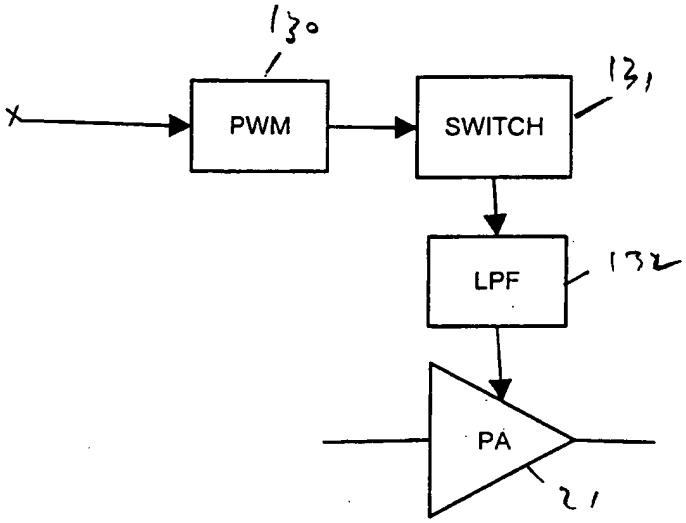

FIGURE 13

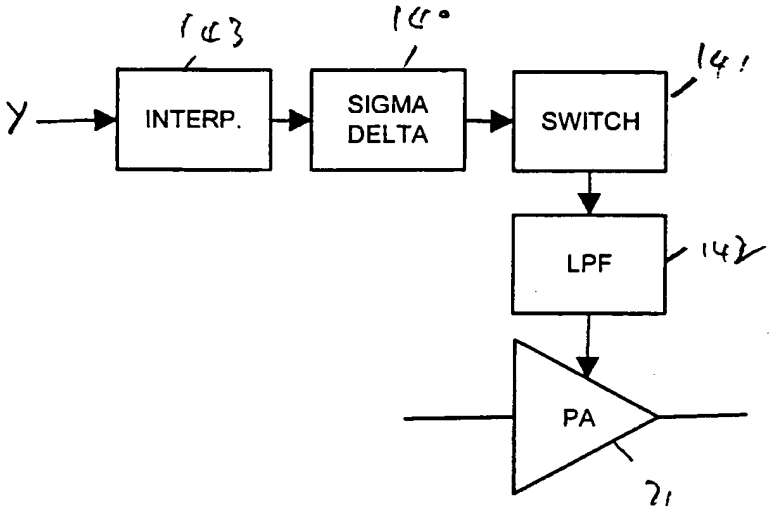

FIGURE 14

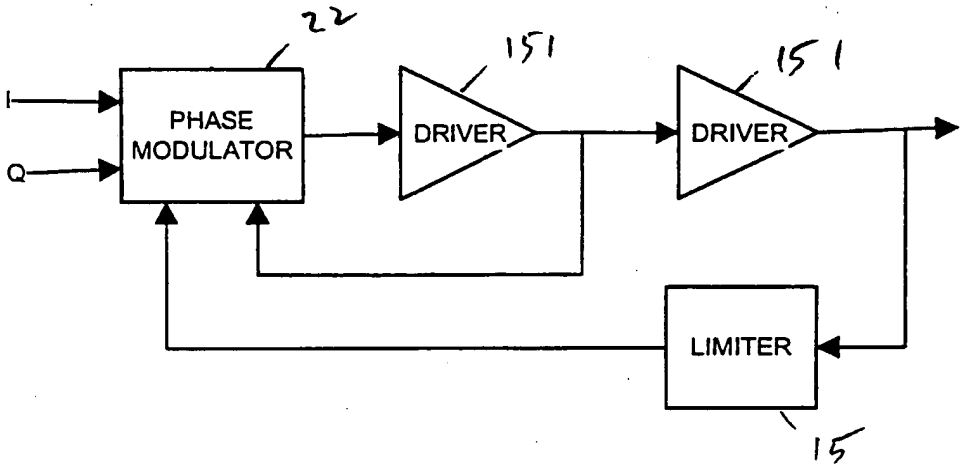

FIGURE 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NZ00/00189

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H03C 5/00, H04L 27/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC GLOBAL

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO 99/54994 A (ROCKWELLSEMICONDUCTOR SYSTEMS, INC.) 28 October 1999 The whole document	1-10
X	EP 360178 A (HUGHES NETWORK SYSTEMS, INC.) 28 March 1990 The whole document	1,2
A	WO 99/05783 A (MOTOROLA, INC.) 4February 1999 The whole document	1-10

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

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Date of the actual completion of the international search
4 January 2001

Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5705959 A (O'LOUGHLIN) 6 January 1998 The whole document	1-10

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/NZ00/00189

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	9954994	US	5966051				
EP	360178	AU	41633/89	CA	1320604	JP	2180453
		US	4972440				
WO	9905783	CN	1234922	DE	19881110	FI	990600
		FR	2766637	GB	2331881	SE	9901094
		US	5886572				
US	5705959	NONE					

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